IPEA
EPO
D-80298 Munich
Germany

1st September 2004

Dear Sirs

PCT/GB01/02774
Our ref: Microarchitecture

Thank you for your Written Opinion dated 1st June 2004. The Opinion is an auto-generated Opinion which states in essence that the invention as claimed lacks novelty and/or inventive step in light of the art cited in the Search Report.

In light of the citations, the applicant files replacement pages as follows:

Replacement pages 24 - 26 to replace the same pages as originally filed.

Triplicate replacement pages will follow with the postal copy of this letter, together with one set of pages marked to show all changes.

Amended Claim 1 of the present application reads:

1. A microprocessor with an architecture incorporating several execution units, whereby:

(a) one or more registers store results from particular execution units;

(b) execution unit operands receive data from one such register;

(c) certain execution units are able to copy data from their operands to result registers; and

(d) the copy capability is used to allow execution units that are not directly connected to communicate data.

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The citations include a limited ability to copy data through the execution unit, but this is not specifically for the purposes of improving the reachability of communication in the architecture. An additional, final clause has been included in the amended Claim 1 to indicate that this is the primary intent of the copy capability. This is not anticipated in the citations.

NOVELTY

US 6 311 261 B1 (CHAMDANI JOSEPH I et al)

This patent provides an extensive survey of the superscalar microprocessor implementations in the early 1990s. It specifically discusses the implementation of reorder buffers that are used to allow out of order issue and completion of instructions in a superscalar processor. Its contribution is an adaptation of such a buffer so that a prioritized associative lookup is not required into the buffer. A suitable keying strategy is used in the reorder buffer so that an element can be uniquely looked up, simplifying and speed up the implementation of the reorder buffer.

The reorder buffer is responsible for arranging the forwarding of data items to the required execution units that are to process a dependent instruction. However, the patent does not discuss in any way the copying of data through the execution units. Data is distributed to the required units directly to the execution units. Thus this citation has low relevance to the present application and does not anticipate the copying through execution units themselves in order to lower connectivity requirements.

US 5 799 163 A (PARK HEONCHUL ET AL)

This describes the register data forwarding arrangement for a superscalar microprocessor. If multiple instructions are to be issued per clock cycle then the maximum number of register file read and write ports required increases. This is undesirable since this increases the area and reduces the operating frequency of the register file. The citation describes an improved mechanism to make use of a reduced number of register files ports allowing a greater number of instruction issues for a given number of ports. Computed data from execution unit may be forwarded directly to a consuming execution

unit. The register file read ports that are rendered redundant by this forwarding may then be redirected to supply operand values to other instructions issued on the cycle.

This citation does not describe the copying of data through the execution units as required by the present application. Although data is forwarded from execution units it will have had computation performed upon it. The present application specifically requires that the data is merely copied unaltered for the purposes of reducing connectivity requirements. The citation requires a full routing network from the register file to the execution units.

US 5 619 664 A (GLEW ANDREW F)

This describes an enhancement to arithmetic computations in a pipeline to increase the level of pipelining and thus the attainable implementation frequency. The principle used is that an intermediate form of a result may be forwarded to a subsequent execution unit and allow the following operation to start. In this example cited the final calculation of the carry bit is delayed into a following pipeline cycle. Other arithmetic operations can be initiated on the intermediate form.

This citation appears to be of low relevance to the present application. There is no discussion of direct copying through an execution unit for the purposes of reducing the connectivity requirements of the architecture. Only intermediate (partially computed) forms of an operation are forwarded, not a direct copy of the original input data.

Should the examiner require further clarification, then a second Written Opinion is requested.

Yours faithfully

Peter Langley